In the Specification

At page 1, lines 5 – 15, please replace the paragraph as follows (underlined denotes replacements additions and strikethough notes deletions):

This Application claims priority for common subject matter to U.S. Provisional Patent Application Serial No. 60/198,365 ~~(AMDA.475P1/TT3991)~~, filed on April 19, 2000 and entitled "Semiconductor Analysis Arrangement and Method Therefor," which is fully incorporated herein by reference. This application is further related to U.S. Patent Application Serial No. 09/838,671 ~~(AMDA.517PA/TT3991P2)~~, now U.S. Patent 6,700,659 entitled "Semiconductor Analysis Arrangement and Method Therefor"; to U.S. Patent Application Serial No. 09/838,667 ~~(AMDA.518PA/TT3991P3)~~, entitled "Semiconductor Analysis Using Thermal Control"; and to U.S. Patent Application Serial No. 09/838,672 ~~(AMDA.519PA/TT3991P4)~~, now U.S. Patent No. 6,635,839 entitled "Semiconductor Analysis Arrangement and Method Therefor," all of which are filed concurrently herewith.

At page 5, lines 20 – 24 and page 6, lines 1 – 13, please replace the paragraph as follows (underlined denotes replacements additions and strikethough notes deletions):

FIG. 1 shows a system 100 for analyzing a semiconductor die 102, according to an example embodiment of the present invention. The system includes a test head 105 adapted to hold the die 102 and to dock with a chamber 110 via a coupling arrangement 140. Once the test head is docked with the chamber, one or more perturbation devices 101, including a light source 106 and other devices, such as a FIB, laser, sonic, microwave, electron beam or ion beam device, is used to analyze the die. Operation control data, such as chamber condition, die response, and other data, is provided to a controller 115. The controller is further adapted to receive response data from the die, such as electrical data obtained from die outputs. The perturbation devices 101 are also optionally coupled to the controller 115, and the controller can be adapted to control and receive feedback from the devices 101. A monitor 120 is coupled to the controller 115 and adapted to display information such as response data, control data. In one particular implementation, the monitor is used as part of an interface for controlling the system 100. For

more information regarding the use of a controller in connection with the present invention, reference may be made to U.S. Patent Application Serial No. 09/838,672 ~~(AMDA.519PA/TT3991P4)~~, now U.S. Patent No. 6,635,839 entitled "Semiconductor Analysis Arrangement and Method Therefor."

At page 7, lines 6 – 19, please replace the paragraph as follows (underlined denotes replacements additions and strikethough notes deletions):

In another example embodiment of the present invention, a photodiode 220 is coupled to the fiber optic cable 210, is communicatively coupled to a controller 280 via communications link 281 and is adapted to detect light leakage from the cable. In response to an amount of light that might leak from the cable, the photodiode generates a signal that is sent to the controller 280. The controller receives the signal and uses it for controlling the analysis of the semiconductor die 275. By detecting light leaking from the fiber optic cable, the corresponding response from the die can be more accurately analyzed because the amount of light incident upon the die can be detected and/or estimated. Any corresponding change in the stimulation or response to the amount of light is accounted for using the detected leakage. In addition, undesirable leakage levels can be avoided. For more information regarding the detection of light leakage, reference may be made to U.S. Patent Application Serial No. 09/838,671 ~~(AMDA.517PA/TT3991P2)~~, now U.S. Patent No. 6,700,659 entitled "Semiconductor Analysis Arrangement and Method Therefor."

At page 8, lines 7 – 20, please replace the paragraph as follows (underlined denotes replacements additions and strikethough notes deletions):

The present invention is adaptable for types of analysis including light induced voltage alteration (LIVA), thermal induced voltage alteration (TIVA), optical beam induced current (OBIC) and critical timing path (CTP) analysis. For more information regarding example types of analysis that can be performed in connection with the present invention, reference may be made to U.S. Patent No. 5,430,305, filed on April 8, 1994 and entitled "Light-induced Voltage Alteration for Integrated Circuit Analysis," to U.S. Patent No. 5,523,694, filed on June 4, 1996

and entitled "Integrated Circuit Failure Analysis by Low-energy Charge-induced Voltage Alteration," to U.S. Patent No. 5,844,416, filed on November 2, 1995 and entitled "Ion-beam Apparatus and Method for Analyzing and Controlling Integrated Circuits," to U.S. Patent Application Serial No. 09/259,542, now U.S. Patent No. 6,177,989 filed on March 1, 1999 and entitled "Laser Induced Current for Semiconductor Defect Detection," and to U.S. Patent Application Serial No. 09/385,775, now U.S. Patent No. 6,541,987 filed on August 30, 1999 and entitled "Laser-excited Detection of Defective Semiconductor Device," which are fully incorporated herein by reference.